

**PCT**

WORLD INTELLECTUAL PROPERTY ORGANIZATION  
International Bureau



INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

<b>(51) International Patent Classification <sup>6</sup> :</b> <b>H01L 21/306</b>	<b>A1</b>	<b>(11) International Publication Number:</b> <b>WO 99/35677</b> <b>(43) International Publication Date:</b> 15 July 1999 (15.07.99)
<b>(21) International Application Number:</b> PCT/US99/00288 <b>(22) International Filing Date:</b> 7 January 1999 (07.01.99)  <b>(30) Priority Data:</b> 09/003,670 7 January 1998 (07.01.98) US  <b>(71) Applicant:</b> QC SOLUTIONS, INC. [US/US]; 150-U New Boston Street, Woburn, MA 01801 (US).  <b>(72) Inventor:</b> KAMIENIECKI, Emil; 18 Stratham Road, Lexington, MA 02173 (US).  <b>(74) Agent:</b> TURANO, Thomas, A.; Testa, Hurwitz & Thibault, LLP, High Street Tower, 125 High Street, Boston, MA 02110 (US).		<b>(81) Designated States:</b> JP, European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE).  <b>Published</b> <i>With international search report. Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments.</i>
<b>(54) Title:</b> APPARATUS AND METHOD FOR RAPID PHOTO-THERMAL SURFACE TREATMENT  <b>(57) Abstract</b>  An apparatus for surface treating a semiconductor wafer includes a surface treatment chamber and a source of radiation. The semiconductor wafer disposed inside the chamber is illuminated with radiation sufficient to create a plurality of electron-hole pairs near the surface of the wafer and to desorb ions and molecules adsorbed on the surface of the wafer.		

**FOR THE PURPOSES OF INFORMATION ONLY**

Codes used to identify States party to the PCT on the front pages of pamphlets publishing international applications under the PCT.

AL	Albania	ES	Spain	LS	Lesotho	SI	Slovenia
AM	Armenia	FI	Finland	LT	Lithuania	SK	Slovakia
AT	Austria	FR	France	LU	Luxembourg	SN	Senegal
AU	Australia	GA	Gabon	LV	Latvia	SZ	Swaziland
AZ	Azerbaijan	GB	United Kingdom	MC	Monaco	TD	Chad
BA	Bosnia and Herzegovina	GE	Georgia	MD	Republic of Moldova	TG	Togo
BB	Barbados	GH	Ghana	MG	Madagascar	TJ	Tajikistan
BE	Belgium	GN	Guinea	MK	The former Yugoslav Republic of Macedonia	TM	Turkmenistan
BF	Burkina Faso	GR	Greece	ML	Mali	TR	Turkey
BG	Bulgaria	HU	Hungary	MN	Mongolia	TT	Trinidad and Tobago
BJ	Benin	IE	Ireland	MR	Mauritania	UA	Ukraine
BR	Brazil	IL	Israel	MW	Malawi	UG	Uganda
BY	Belarus	IS	Iceland	MX	Mexico	US	United States of America
CA	Canada	IT	Italy	NE	Niger	UZ	Uzbekistan
CF	Central African Republic	JP	Japan	NL	Netherlands	VN	Viet Nam
CG	Congo	KE	Kenya	NO	Norway	YU	Yugoslavia
CH	Switzerland	KG	Kyrgyzstan	NZ	New Zealand	ZW	Zimbabwe
CI	Côte d'Ivoire	KP	Democratic People's Republic of Korea	PL	Poland		
CM	Cameroon	KR	Republic of Korea	PT	Portugal		
CN	China	KZ	Kazakhstan	RO	Romania		
CU	Cuba	LC	Saint Lucia	RU	Russian Federation		
CZ	Czech Republic	LI	Liechtenstein	SD	Sudan		
DE	Germany	LK	Sri Lanka	SE	Sweden		
DK	Denmark	LR	Liberia	SG	Singapore		
EE	Estonia						

## **APPARATUS AND METHOD FOR RAPID PHOTO-THERMAL SURFACE TREATMENT**

### **FIELD OF THE INVENTION**

The invention relates to an apparatus and method for processing a semiconductor, and more specifically, relates to an apparatus and method for surface treating a semiconductor wafer in preparation for an in-line monitoring procedure.

### **BACKGROUND OF THE INVENTION**

5        Operation of an integrated circuit (IC) depends on the electrical properties of materials of which the circuit is formed. Therefore, by monitoring selected electrical properties of these materials in the course of an IC fabrication, an effective control over the manufacturing process can be accomplished. Since modern ICs are typically formed in the shallow region below the surface of a semiconductor wafer, critical electrical properties are directly or indirectly related to  
10    the condition of the surface region of the semiconductor wafer. Surface properties of a semiconductor wafer can be monitored during IC fabrication through in-line monitoring procedures such as described in U.S. Pat. No. 4,544,887 and U.S. Pat. No. 5,661,408.

The in-line monitoring procedure permits surface properties of a semiconductor wafer to be measured without contacting the wafer surface, so that the surface properties are not affected  
15    by the measurement itself. However, unlike conventional methods of electrical characterization in which contaminant ions and molecules from the ambient environment do not significantly affect the measurements due to formation of a permanent contact on the surface of the wafer, non-contact measurements may not provide accurate information about the wafer. This is because contaminant ions and molecules from the ambient environment may adsorb on the surface of the  
20    wafer during transportation and storage, changing surface properties of the wafer. Consequently,

- 2 -

it may be difficult to obtain accurate information about the surface properties of the semiconductors with the in-line monitoring procedures unless the semiconductors are surface treated prior to being measured.

According to one known method, a p-type silicon wafer is surface treated by being  
5 immersed in dilute hydrofluoric acid, rinsed with deionized water and dried in order to restore an inversion condition. A width of surface depletion layer measured under an inversion condition provides net doping concentration in the sub-surface region. Existing surface preparation steps, however, are typically not integrated with subsequent measurement steps. In addition, existing processing and monitoring methods are not capable of establishing the surface condition of a  
10 wafer by means of a simple treatment in ambient environment at atmospheric pressure as needed to carry out a specific electrical measurement.

Therefore, there is a need for an apparatus and method which determine selected electrical parameters of semiconductor wafers representing the outcome of individual processing steps, independent of the ambient atmosphere in which the wafers are stored or transported.

15

#### SUMMARY OF THE INVENTION

It is an object of the invention to provide a surface treatment apparatus and method, which reduce the affect of ambient environment, in which a wafer is transported or stored between processing steps, on the wafer surface condition. It is another object of the invention to provide a surface treatment apparatus and method which can be integrated with an in-line monitoring  
20 apparatus and method.

In one aspect, the invention features a method for in-line, real-time monitoring of a semiconductor wafer. According to the method, a plurality of electron-hole pairs are created near a surface of the wafer and the wafer is heated to substantially desorb any of a plurality of

- 3 -

contaminant ions and molecules adsorbed on the surface of the wafer. In one embodiment, the plurality of electron-hole pairs are created by illuminating the wafer with a radiation of photon energy sufficient to create the plurality of electron-hole pairs. In another embodiment, the wafer is heated by illuminating the wafer with a near infrared radiation. In still another embodiment, the  
5 wafer is a p-type wafer and heating and illuminating the p-type wafer restores an inversion layer on the surface of the p-type wafer.

In another aspect, the invention features an apparatus for surface treating a semiconductor wafer. The apparatus includes a surface treatment chamber and a source of radiation, which illuminates a semiconductor wafer disposed inside the chamber with radiation sufficient to create a  
10 plurality of electron-hole pairs near a surface of the wafer and to desorb any of a plurality of ions and molecules adsorbed on the surface of the wafer. In one embodiment, the surface treatment chamber is integrated with an in-line, real-time testing apparatus such that a surface photovoltage of the wafer can be measured after the wafer has been surface treated. In another embodiment, the apparatus further comprises a power control circuitry for controlling an intensity of radiation  
15 from the radiation source.

- 4 -

BRIEF DESCRIPTION OF THE DRAWINGS

The invention is pointed out with particularity in the appended claims. The above and further advantages of this invention may be better understood by referring to the following description taken in conjunction with the accompanying drawings, in which:

5       FIG. 1 is a graph illustrating time dependence of a surface charge measured on a p-type CZ silicon wafer sequentially exposed to clean room air, stored in a box and exposed again to clean room air.

10       FIG. 2 is a graph illustrating time dependence of a surface charge measured on an n-type CZ silicon wafer sequentially stored in a box, exposed to clean room air, and again stored in a box.

FIGS. 3a-e illustrate adsorption of contaminant ions and molecules from the ambient environment on a surface of a semiconductor wafer and desorption of the contaminant ions and molecules from the wafer surface through a subsequent photo-thermal treatment of the invention.

15       FIG. 4 is a graph comparing the surface charges of two p-type silicon wafers grown in the same batch, one as-grown and the other RCA cleaned (SC1+SC2), immediately after fabrication, after storage for 12 weeks, and after photo-thermal treatment.

FIG. 5 is a schematic diagram of an embodiment of an apparatus of the invention for photo-thermal surface treatment of a semiconductor wafer.

20       FIG. 6 is a graph illustrating dependence of electrical characteristics of two p/p+ silicon epitaxial wafers on peak temperature during photo-thermal treatment at constant processing time of 30 seconds.

- 5 -

FIG. 7 is a graph comparing deviations of the apparent doping concentration measured in as-grown p-type silicon wafers before and after photo-thermal treatment at peak temperature of 250°C.

FIG. 8 is a graph comparing deviations of the apparent doping concentration measured in  
5 RCA cleaned p-type silicon wafers before and after photo-thermal treatment at peak temperature of 250°C.

#### DESCRIPTION OF THE PREFERRED EMBODIMENT

The surface condition of a semiconductor wafer depends on surface preparation as well as the wafer's surrounding ambient environment, which may be in gaseous, vapor, or liquid phase.

10 In general, surfaces of semiconductor wafers tend to reach equilibrium with the surrounding ambient environment. Therefore, ions and molecules present in the ambient environment may adsorb to surfaces of the wafers exposed to the ambient environment, and changes in the ambient environment composition will also cause changes in the layer adsorbed to the surface. The effect of the gaseous ambient environment on the surfaces of wafers have been recognized and utilized  
15 by those skilled in the art, for example, as a means of varying the surface potential barrier height in germanium.

Referring to Figures 1 and 2, the surface charge in silicon wafers varies as the ambient environment changes. Figure 1 shows surface charge variation in a p-type wafer as a function of time and storage conditions. In Figure 1, the p-type wafer is first exposed to a clean room air for  
20 approximately 70 minutes, stored in a covered box for approximately 800 minutes, and again exposed to the clean room air for approximately 225 minutes. The surface charge in the p-type wafer is measured using the surface photo-voltage method as described in U.S. Pat. No. 4, 544,887 issued on Oct. 1, 1985 and U.S. Pat. No. 5, 661,408 issued on Aug. 26, 1997, both

- 6 -

assigned to the assignee of the present invention. Figure 2 similarly shows surface charge variation in an n-type wafer. In Figure 2, the n-type wafer is sequentially stored in a box for approximately 740 minutes, exposed to clean air for approximately 300 minutes, and again stored in a box for approximately 300 minutes. The surface charge of the n-type wafer is also derived from surface photo voltage measurements. The surface charge measurements shown in Figures 1 and 2 demonstrate the sensitivity of the silicon surface charge to the clean-room and the storage container ambient environment conditions. While the magnitude of the surface charge variations for p-type and n-type wafers as shown in Figures 1 and 2 differs, the polarity of the changes is the same, independent of the conductivity type of the wafer. Exposure to clean-room air results in more negative surface charges and storage in the container results in more positive charges forming at the wafer surface. The difference in the polarity of the surface charge changes can be attributed to the difference in the composition of the clean-room and the box ambient environments. It has been observed by the inventor that the rate of change in the surface charge depends on the surface preparation, and composition of water-based cleaning solutions used in cleaning the wafers.

Figures 3 (a-e) show an evolution of the contamination of a silicon wafer surface due to its interaction with a surrounding environment. A crystalline silicon wafer (Fig. 3a) has a positive charge associated with the lack of bonds to atoms at the wafer surface as symbolically illustrated in Fig. 3a. However, such an abruptly terminated surface is inherently unstable, and other species from the surrounding ambient environment will adsorb on the surface of the wafer. The atoms in a few top monolayers of the silicon crystal may also rearrange their configuration resulting in a more gradual transition from the surface to the bulk crystalline



- 7 -

structure. In this case, the positive charge associated with the crystal termination will be distributed across a few top monolayers.

The stability of such bare silicon surface will depend on its prior history. However, given enough time, the exposure of the silicon surface to the surrounding environment will result in the formation of a thin native oxide layer 14 as illustrated in (Fig. 3b). Similarly, a thin chemical oxide film could be formed on the silicon wafer surface 12 when the wafer is subjected to a cleaning procedure, such as an RCA clean. The positive charge at a wafer surface associated with crystal termination will spread into the oxide in both cases. However, as illustrated in Fig. 3b, negative ions 16 from the ambient environment can interact with the wafer surface 12 during or before oxide formation. These interactions with negative ions 16 from the ambient environment may result in adsorption of these species to the surface of the wafer 12 with the resulting contamination of the native or chemical oxide layer 14. Negative ions 16 from the ambient environment reduce positive oxide charge. Examples of such contaminants, in the case of the RCA clean, are aluminum and iron.

Neutral polar molecules 18 from the liquid ambient environment (e.g., water or alcohol) may adsorb on the oxide layer 14 of the wafer surface 12, resulting in formation of a double-layer 20 as shown in Fig. 3c. The double-layer 20 can also result from adsorption of polar molecules 18 from the air (Fig. 3c). The double layer may also contain some negative ions and species 22, 24, again reducing positive charge at the surface of the wafer. It can be expected that the transition from the virgin surface (shown in Fig. 3a) to a double-layer 20 coated surface (Fig. 3c) will take longer than transition from the oxidized surface 14 (Fig. 3b) to the double-layer 20 coated surface Fig. 3c. This principle is illustrated in Figure 4, which compares evolution of two p-type silicon epitaxial wafers grown in the same batch, during storage and after photo-thermal

- 8 -

surface treatment. One wafer, labeled as "as-grown", was not subject to any cleaning, while the other wafer, labeled "SC1+SC2", was subject to an oxidizing clean. The graph in Figure 4 shows that the surface charge of the two wafers immediately after removal from the shipping containers is already substantially different, and both deviate from the target surface charge represented by a dash line. The RCA-treated wafer shows less positive charge than the as-grown wafer. The difference between the wafers increase even more after the wafers are stored in a container for further 12-weeks, illustrating that charge variation in RCA-treated wafer occurs faster than in a non-treated wafer. The graph in Figure 4 also shows that photo-thermal surface treatment of the present invention restore the positive surface charge on both wafers approximately to the target value.

Referring to Figure 3d, the present invention features a photo-thermal surface treatment method and an apparatus for removing or neutralizing surface charges associated with the double layer 20. According to the invention, a plurality of electron-hole pairs 30 are created near the surface of the wafer 12 by illuminating the wafer. Creation of the electron-hole pairs 30 weakens the strength with which non-volatile ions and molecules of the double layer 20 are adsorbed to the oxide layer 14. The wafer is also heated to substantially desorb volatile contaminant ions and molecules adsorbed on the surface of the wafer 12. As the volatile contaminant ions and molecules, including polar molecules 18 forming a double layer 20 desorb, they carry away the non-volatile contaminant ions and molecules 22, 24 as well. Therefore, after photo-thermal surface treatment, the surface charge properties of the wafer is returned to its state prior to formation of the double layer 20 as shown in Fig. 3e.

In the case of p-type silicon wafers, the positive surface charge induces an inversion condition at the surface by repelling positively charged free holes from the surface region.

- 9 -

Therefore, the photo-thermal surface treatment restoring the positive surface charge will also restore inversion conditions at the surface. This allows the establishment of reference conditions at the semiconductor surface for the measurement of the basic electrical parameters such as doping concentration and surface recombination lifetime. The photo-thermal surface treatment of p-type silicon wafers may also allow activating of dopants such as boron, which were deactivated due to interaction with hydrogen or metal atoms.

The invention makes use of optical radiation 32 (Fig. 3d) under defined conditions to remove species adsorbed on the surface 12 of a semiconductor wafer 11 due to interaction with an ambient environment. In this method, a uniform beam of light 32 is directed at the surface 12 of the semiconductor wafer 11, illuminating the wafer 11. The illuminating light 32 comprises a combination of short and long wavelength light. The short wavelength light has wavelengths greater than that corresponding to the energy gap of the semiconductor material. The long wavelength light has wavelength in the near infrared range. The light with the wavelength greater than the band gap generates a high density of free electrons and holes 30 (Fig. 3d) near the semiconductor surface 12 and heats the wafer 11. The light in the near infrared range further increases the temperature of the semiconductor surface 12 to that required to desorb or evaporate volatile molecular species adsorbed on the surface 12. As the volatile species desorb, they carry away other, non-volatile ions and molecules adsorbed to the surface 12 of the wafer 11.

The effect of photo-thermal surface treatment of a wafer can be monitored by measuring the AC surface photovoltage of the wafer under conditions disclosed in U.S. Pat. No. 4,544,887 and U.S. Pat. No. 5,661,408. The conditions of the wafer treatment, temperature and illumination time are determined based on these measurements.

- 10 -

Referring to Fig. 5, an apparatus for photo-thermal surface treatment includes two major parts: a wafer-processing module 40 and a power control circuitry 42. The wafer-processing module 40 includes a light source unit 44 integrated with the wafer processing chamber 46. The light source unit 44 is capable of generating light having wavelengths sufficient to generate free electron-hole pairs near the surface of the wafer and near infrared light. In the embodiment of Fig. 5, the light is provided by tungsten halogen quartz lamps 48. The lamps 48 provide the light in the spectral range from about 0.2 $\mu$ m to about 4  $\mu$ m. The lamps 48 are mounted to a water-cooled top light reflector 52 with ceramic lamp supports 50. In an alternative embodiment, a hot plate or a furnace is used to heat the wafer, while the light source provides the short wavelengths light. The wafer is heated to a temperature in the range from about 200°C to about 300°C. The top light reflector 52 includes a series of parabolic reflectors 53 which provide uniform illumination over the entire wafer located in the processing chamber 46.

In one embodiment, the light source 44 may comprise 10 tubular quartz halogen lamps of 1000 Watts each. In this embodiment, the distance between the lamps may be approximately 20 mm. To compensate for the decrease in light intensity at the periphery of the illuminated area, the water-cooled side reflectors 54 are added on all four sides of the process chamber 46. Alternatively, these four side reflectors 54 may be replaced by a cylindrical reflector with a diameter slightly exceeding the diameter of the wafer 56. The diameter of the cylindrical reflector, for example, may exceed the diameter of the wafer 56 by about 20 mm. The side reflectors 54 extend below the plane of wafer 56, when the wafer 56 is disposed on a wafer support 58 in the process chamber 46.

The apparatus further includes a water-cooled bottom light reflector 60 under the wafer 56 to improve the uniformity of the light. In one embodiment, the wafer 56 is supported by three

- 11 -

thermally insulating pins 58 manufactured from Vespel® provided by DuPont Company (Wilmington, Delaware) arranged in a triangular configuration. The top, side and bottom light reflectors 52, 54, 60 form a "black-body" box, uniformly illuminating the chamber 46 due to multiple scattering. Light uniformity in the embodiment of Figure 5 has been measured. At the  
5 distance of about 100 mm below the lamps 48, the light uniformity was  $\pm 5\%$  across an area 200 mm in diameter. The distance of 100 mm below the lamps 48 corresponds to wafer location.

In the embodiment of Figure 5, the power control circuitry 42 is in communication with the wafer-processing module 40 in a closed-loop. The intensity of light illuminating the wafer 56 is controlled by measuring radiation from the wafer 56 with an infrared sensor 62 located beneath  
10 the wafer 56. In one detailed embodiment, the sensor 62 is located about 25 mm beneath the wafer 56. The radiation information is used to control the intensity of light illuminating the wafer 56.

The infrared sensor 62 is sensitive only to the radiation of wavelengths between  $6.5 \mu\text{m}$  and  $14 \mu\text{m}$ , and therefore, measures radiation emitted by the wafer 56 and not the light source 44.  
15 The signal from the infrared sensor 62 is fed into a lamp power controller 74 which controls power supplied to the lamps 48, and hence controls intensity of the light illuminating the wafer 56. The controller 74 is programmed manually or via a connection to a computer 72 for the wafer 56 to reach a predetermined temperature and then to maintain this temperature for a predetermined time.

20 To provide accurate measurement of the wafer temperature, the wafer-processing module 40 further includes a set of optical filters 64, 66 made of quartz. The set of optical filters 64, 66 filters infrared radiation from the lamps 48 exceeding wavelength of approximately  $4 \mu\text{m}$ , such that the temperature detected by the sensor 62 results from the wafer radiation only. The first

- 12 -

quartz filter 64 absorbs light having wavelength exceeding about 4  $\mu\text{m}$ . The absorption of light causes this filter 64 to warm up and to emit infrared radiation of wavelengths longer than 4  $\mu\text{m}$ . This radiation is subsequently absorbed by the second quartz filter 66. The quartz filters 64, 66 are cooled down by air passing through a passageway 68 between the filters 64, 66. In one  
5 embodiment, an electrical fan forces air through the inlet 70 of the passageway 68.

The light source 44, in combination with the filters 64, 66 produce light having wavelengths of less than about 4  $\mu\text{m}$ . This light illuminating the wafer 56 is capable of generating free electron-hole pairs near the surface of the wafer and heating the wafer to a temperature sufficient to desorb contaminant ions and molecules. The radiation emitted by the heated wafer  
10 56 is measured using the infrared sensor 62.

After completion of the illumination cycle, the power applied to the lamps 48 is turned off and the wafer 56 is left to cool down to a room temperature. Alternatively, the three wafer support pins 58 can be retracted causing the wafer 56 to get in a close proximity or touch the water cooled bottom reflector 60 to speed up the wafer cooling process. During the cooling  
15 process, the temperature of the wafer 56 is again monitored by the infrared sensor 62. Once the wafer 56 is cooled to a temperature close to a room temperature (within about 5°C), the wafer 56 is moved from the cooling station back to the cassette or to the surface measuring station.

A benefit of the photo-thermal surface treatment apparatus is that the surface treatment apparatus may be integrated with an in-line, real-time testing apparatus, such that electric  
20 characteristics of the surface treated wafers can be measured. For example, AC photovoltage induced at the surface of the wafers can be measured and analyzed.

Electrical characteristics of p-type wafers, photo-thermal surface treated at various temperatures, have been measured. AC photovoltage induced at the surface of the wafers have

- 13 -

been measured and analyzed with a method described in U.S. Pat. No. 4,544,887 and U.S. Pat. No. 5,661,408. Carrier lifetime, doping concentrations, conductivity type and depletion width have been determined from the surface photovoltage measurements. Referring to Fig. 6, electrical characteristics of p-type epitaxial layers depend on the maximum or peak temperature reached by the wafer during the illumination cycle. In the embodiment of Fig. 6, the time required to reach the peak temperature during treatment was about 30 seconds. Immediately after reaching the peak temperature, the illumination was turned off and the wafer was permitted to cool. Wafers were measured at room temperature after each heating-cooling cycle.

The surface charge,  $Q_s$  [ $q/cm^2$ ], and the reciprocal of the surface recombination lifetime,  $1/\tau$  [ $1/\mu sec$ ], were measured for two p/p+ silicon epitaxial wafers with epitaxial layer resistivities of 1.4 ohm-cm and 30 ohm-cm, respectively. The surface charge of the wafers increased after each heating-cooling cycle, reversing the change in surface charge due to exposure to the clean-room air for about 2 hours. With further increase in temperature, the surface charge reached its saturation value corresponding to the surface inversion. Similarly, the reciprocal of the surface recombination lifetime changed with the processing conditions, reaching saturation at about the same temperature as the surface charge. The same dependence on processing conditions was observed independent of the resistivity of the wafer and wafer cleaning. This is demonstrated in Figure 4, which shows two epitaxial wafers, one as-grown and one SC1+SC2 treated, both reaching about the same target value after photo-thermal treatment. For temperatures exceeding the temperature at which the surface charge and the reciprocal of the surface recombination lifetime reached the saturation value, further illumination beyond the time required to reach a peak temperature did not affect the measurements. At lower temperatures, the measured values increased slightly with increased illumination time.

- 14 -

In general, processing conditions required to reach saturation depends on wafer parameters. They depend, for instance, on the wafer diameter and thickness. They may be different for CZ and epitaxial wafers. A wafer coating (e.g., thermal oxide coating) is also expected to change treatment conditions.

5 Photo-thermal treatment restores positive surface charge and inversion conditions, which allows the establishment of reference conditions for determining specific parameters of the wafers. Two important parameters include near surface doping concentration,  $N_{sc}$ , and surface recombination lifetime,  $\tau$ . These parameters can be determined from the measurement of the AC surface photovoltage performed under conditions as described in U.S. Pat. No. 4,544,887 and  
10 U.S. Pat. No. 5,661,408.

Referring to Fig. 7, the apparent doping concentrations of as-grown p-type silicon epitaxial wafers before and after photo-thermal treatment at peak temperature of 250°C are compared. The abbreviation PTT refers to photo-thermal treatment. The doping concentrations were measured with an assumption that each wafer surface was at inversion. For all measured  
15 wafers, the apparent doping concentrations deviated from a target value more before photo-thermal treatment then after the treatment. The values after surface treatment were within expected wafer batch uniformity.

Referring to Fig. 8, doping concentrations of RCA cleaned p-type silicon epitaxial wafers are compared before and after photo-thermal treatment at peak temperature of 250°C. The  
20 measurement conditions were the same as for the wafers of Fig. 7. The measured doping concentrations deviated from a target value more before photo-thermal treatment then after. The deviation before photo-thermal treatment was about an order of magnitude higher than for the RCA cleaned epitaxial wafers than for the as grown wafers shown in Fig. 7.



- 15 -

Having shown the preferred embodiment, those skilled in the art will realize many variations are possible, which will still be within the scope and spirit of the claimed invention. Therefore, it is the intention of the applicant to limit the invention only as indicated by the scope of the following claims.

- 16 -

## CLAIMS

We claim:

- 1 1. A method for in line, real-time processing and monitoring of a semiconductor wafer  
2 comprising:  
3 creating a plurality of electron-hole pairs near a surface of the wafer; and  
4 heating the wafer to substantially desorb any contaminant adsorbed on the surface of the  
5 wafer.
- 1 2. The method of claim 1 wherein creating a plurality of electron-hole pairs comprises  
2 illuminating the wafer with radiation sufficient to create a plurality of electron-hole pairs near the  
3 surface of the wafer.
- 1 3. The method of claim 2 wherein heating the wafer comprises illuminating the wafer with a  
2 near infrared radiation.
- 1 4. The method of claim 2 wherein heating the wafer comprises placing the wafer on a hot  
2 surface.
- 1 5. The method of claim 2 further comprising automatically controlling intensity and duration  
2 of heating and illuminating steps.
- 1 6. The method of claim 2 further comprising measuring a temperature of the wafer during  
2 the heating step and controlling intensity and duration of heating and illuminating steps based on  
3 the measured temperature.
- 1 7. The method of claim 2 wherein the wafer is heated and illuminated until a stable surface  
2 condition is achieved.
- 1 8. The method of claim 1 wherein heating comprises heating the substrate to a temperature  
2 in the range from about 200 °C to about 300 °C.

- 17 -

- 1 9. The method of claim 3 wherein illuminating with a near infrared radiation comprises  
2 illuminating with light having a wavelength in the range from about 0.2 microns to about 0.4  
3 microns.
- 1 10. The method of claim 2 further comprising cooling the wafer after heating and illuminating  
2 the wafer.
- 1 11. The method of claim 2 wherein the wafer is a p-type wafer and heating and illuminating  
2 the wafer restores an inversion layer at the surface of the p-type wafer.
- 1 12. The method of claim 2 wherein the wafer is a p-type wafer and heating and illuminating  
2 the wafer activates dopants previously deactivated due to interactions with contaminant ions.
- 1 13. The method of claim 1 further comprising:  
2 illuminating a portion of the wafer with a modulated light; and  
3 measuring an electrical characteristic of the wafer.
- 1 14. The method of claim 13 wherein measuring an electrical characteristic comprises  
2 measuring a photovoltage induced at the surface of the wafer.
- 1 15. The method of claim 14 further comprising calculating a carrier lifetime from the  
2 measured surface photovoltage.
- 1 16. The method of claim 14 further comprising determining a conductivity type from the  
2 measured surface photovoltage.
- 1 17. The method of claim 14 further comprising determining a doping concentration from the  
2 measured surface photovoltage.
- 1 18. An apparatus for surface treating a semiconductor wafer comprising:  
2 a surface treatment chamber; and

- 18 -

3       a source of radiation illuminating a semiconductor wafer disposed inside the chamber with  
4       a radiation sufficient to create a plurality of electron-hole pairs near a surface of the wafer and to  
5       desorb any contaminant adsorbed on the surface of the wafer.

1       19.     The apparatus of claim 18 wherein the surface treatment chamber is integrated with an in-  
2       line, real-time testing apparatus, such that electrical characteristics of the wafer can be measured.

1       20.     The apparatus of claim 19 wherein a surface photovoltage of the wafer is measured after  
2       the wafer has been surface treated.

1       21.     The apparatus of claim 18 wherein the source of radiation comprises a tungsten halogen  
2       quartz lamp.

1       22.     The apparatus of claim 18 further comprising a plurality of reflectors disposed inside the  
2       surface treatment chamber to provide uniform illumination of the wafer.

1       23.     The apparatus of claim 18 further comprising a power control circuitry for controlling an  
2       intensity of radiation from the radiation source.

1       24.     The apparatus of claim 18 further comprising a temperature sensor for monitoring  
2       radiation from the wafer during surface treatment.

1       25.     The apparatus of claim 18 further comprising a filter disposed between the radiation  
2       source and the wafer for filtering radiation having wavelength greater than about 4 microns.

1       26.     The apparatus of claim 18 further comprising a first filter disposed between the radiation  
2       source and the wafer, a second filter disposed adjacent the first filter, and an air passageway  
3       disposed between the first filter and the second filter for cooling the filters, wherein the first filter  
4       and the second filter prevents radiation having wavelengths greater than about 4 microns from  
5       reaching the wafer.

1/8

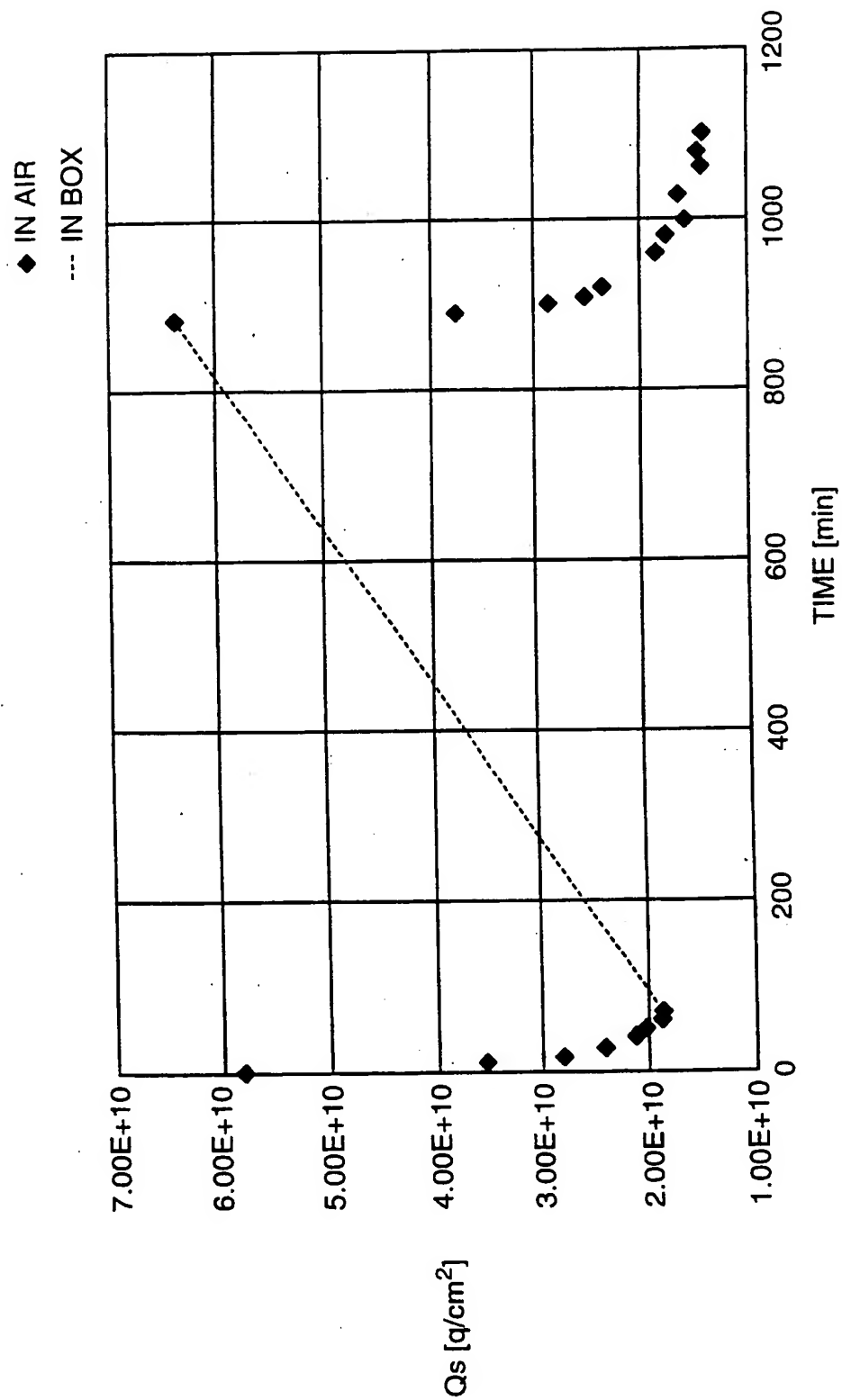


FIG. 1

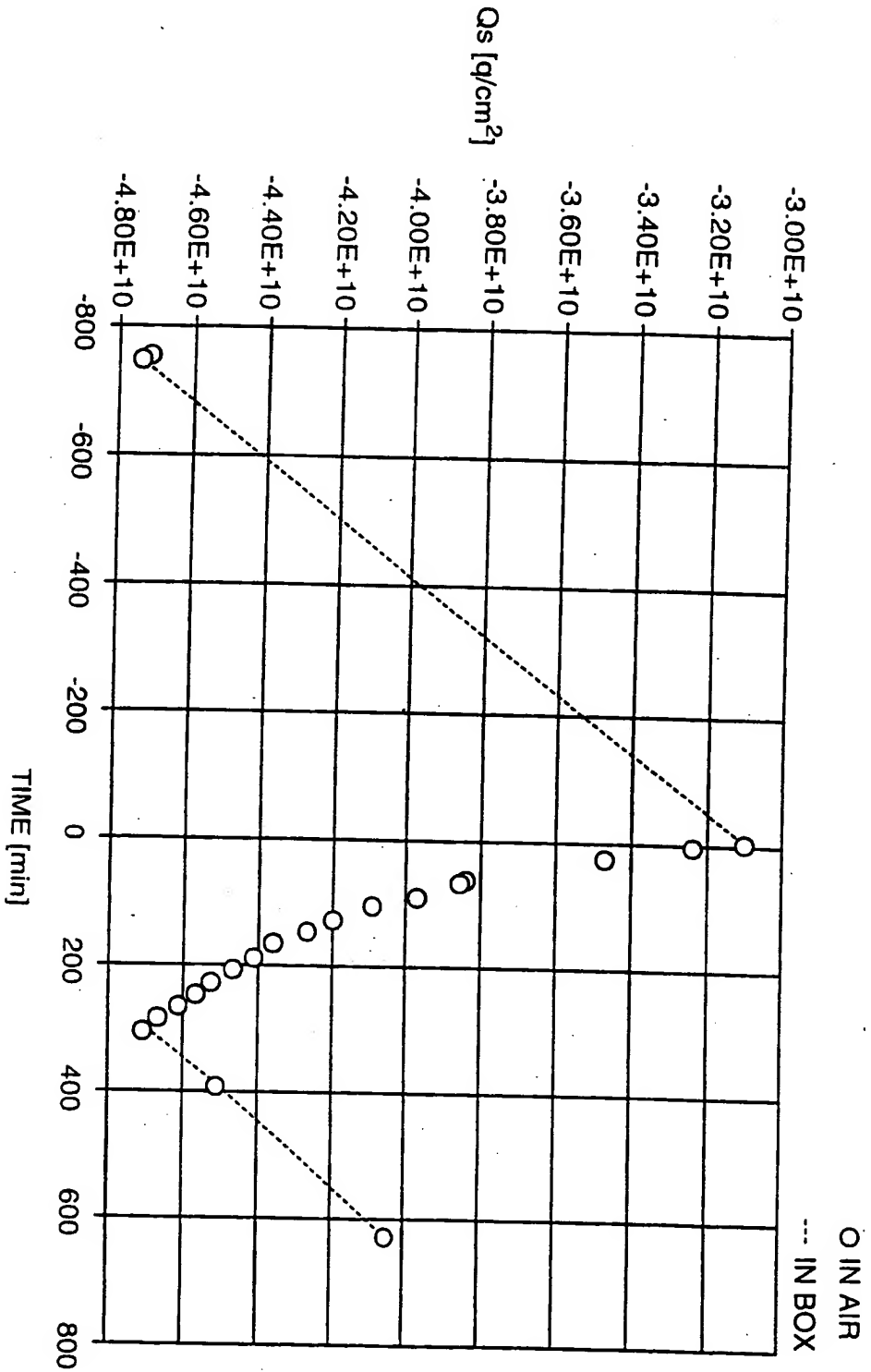


FIG. 2

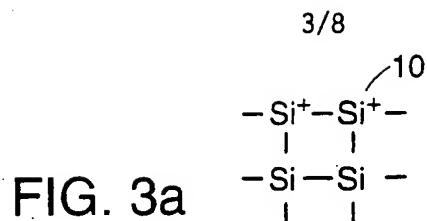


FIG. 3b

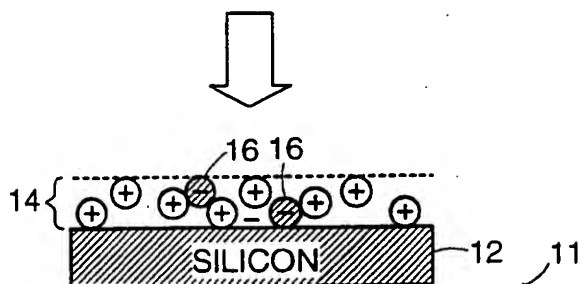


FIG. 3c

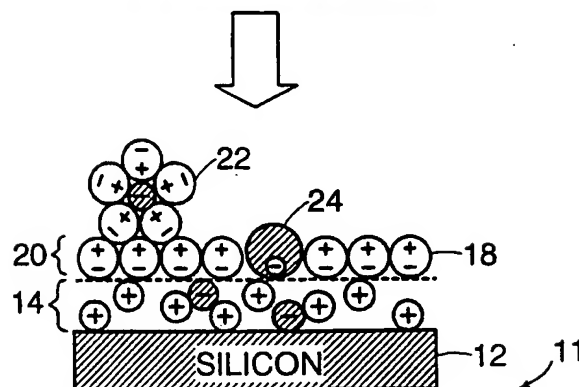


FIG. 3d

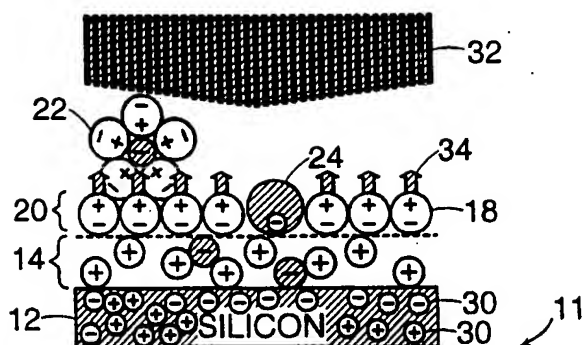
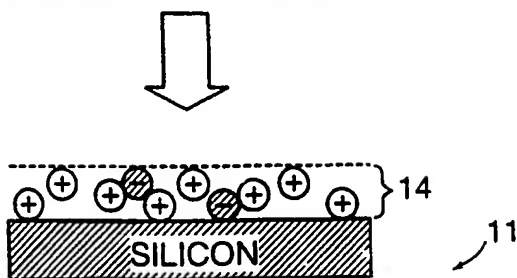


FIG. 3e



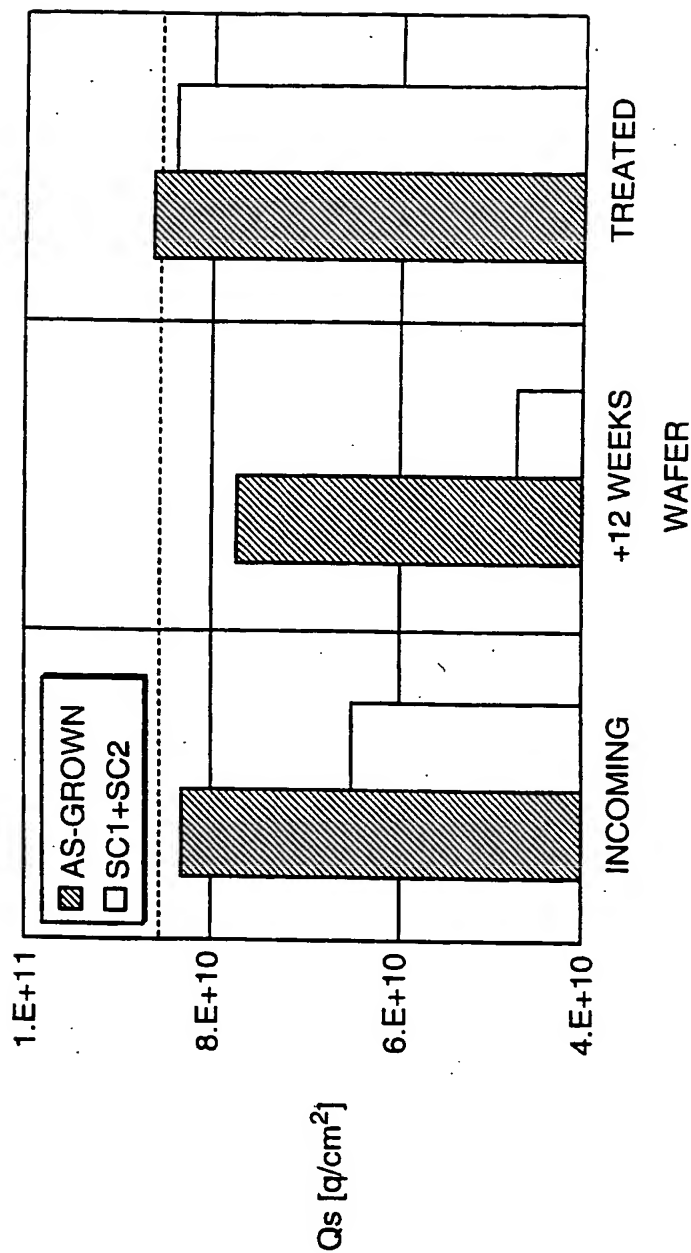


FIG. 4



5/8

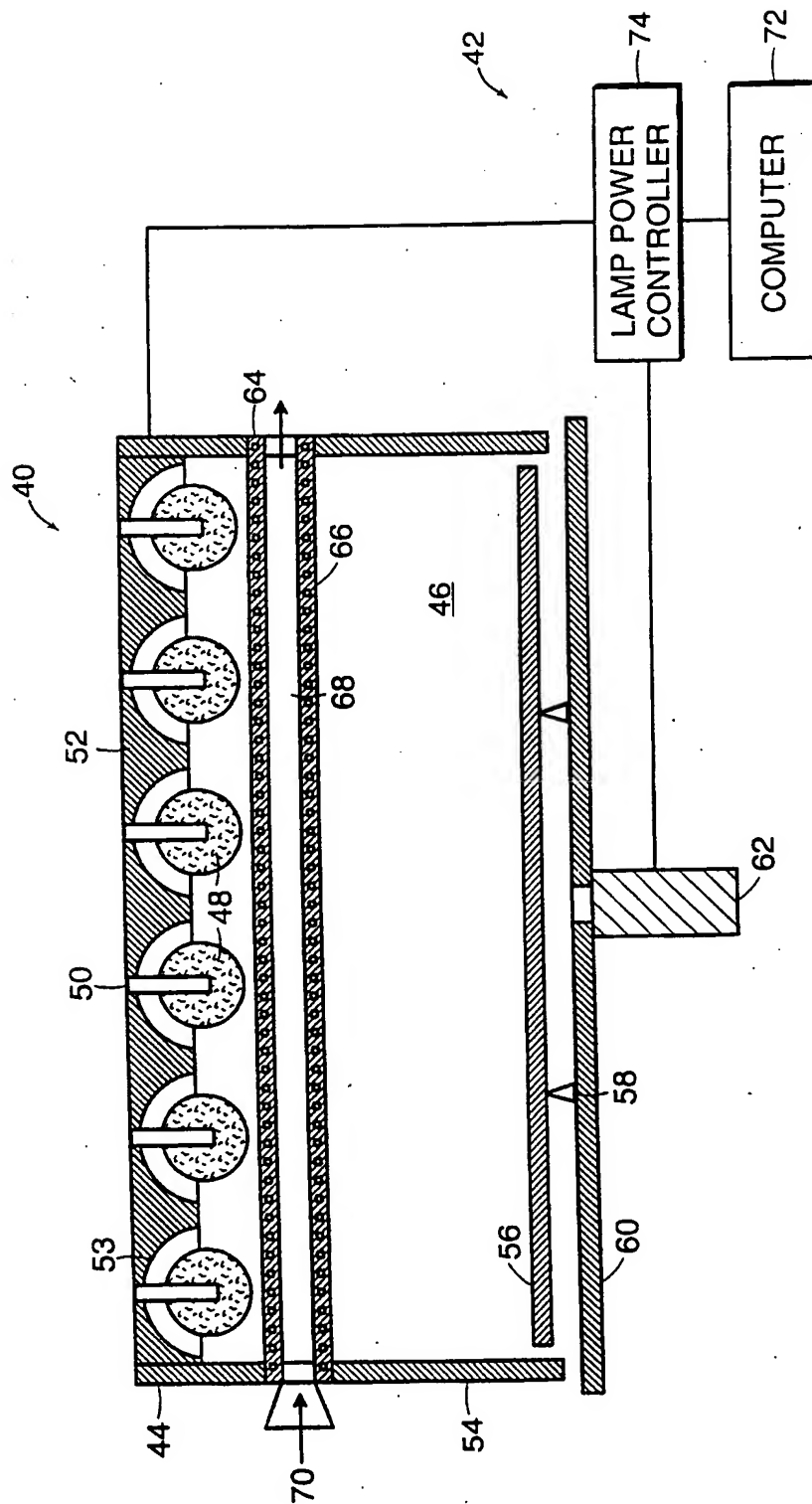


FIG. 5

6/8

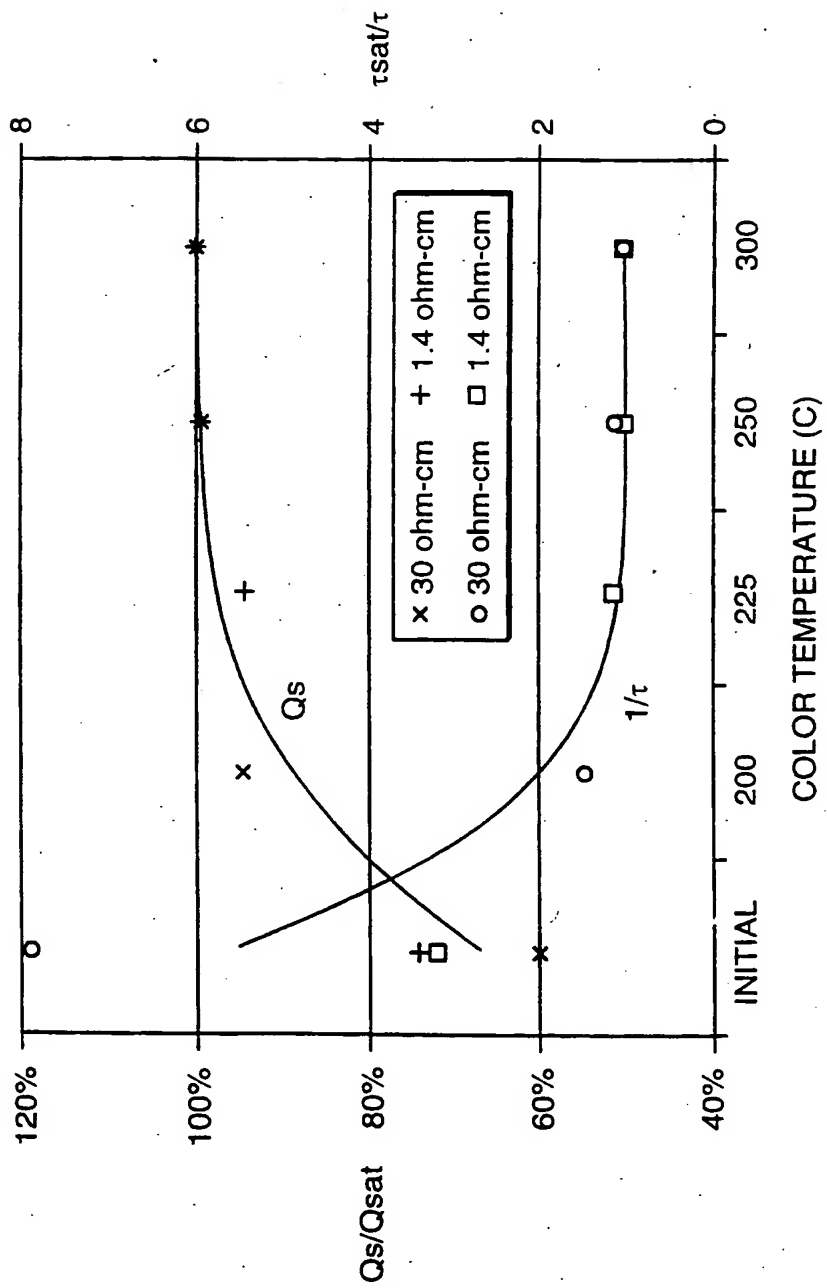


FIG. 6

7/8

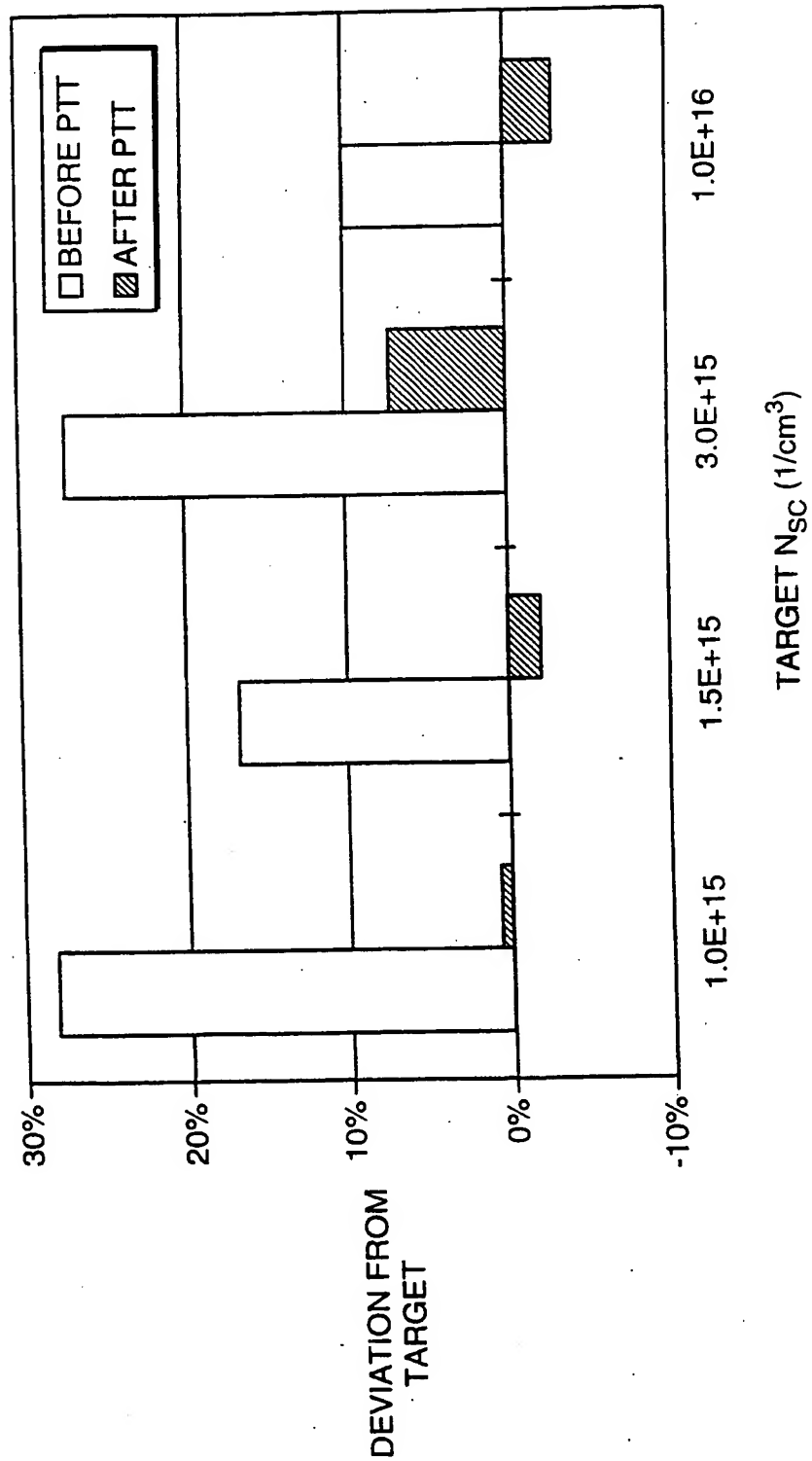


FIG. 7

8/8

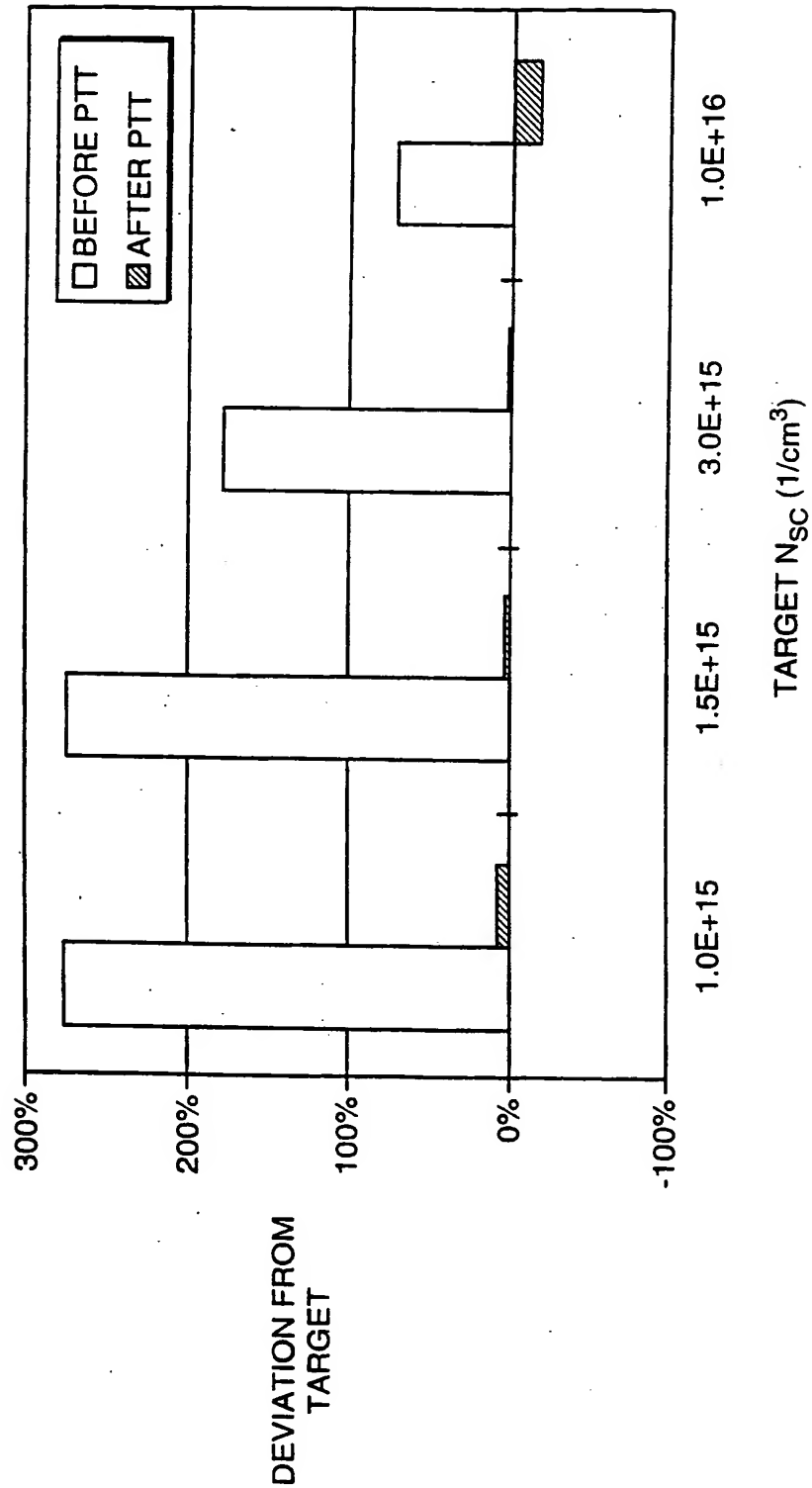


FIG. 8

# INTERNATIONAL SEARCH REPORT

International Application No  
PCT/US 99/00288

**A. CLASSIFICATION OF SUBJECT MATTER**  
IPC 6 H01L21/306

According to International Patent Classification (IPC) or to both national classification and IPC

**B. FIELDS SEARCHED**

Minimum documentation searched (classification system followed by classification symbols)

IPC 6 H01L B08B

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	DE 41 22 587 A (MITSUBISHI ELECTRIC CORP) 23 January 1992 see column 2, line 39 - line 64 see column 3, line 43 - column 7, line 35	1,3,8,18
A	AKAZAWA H ET AL: "PHOTOSTIMULATED EVAPORATION OF SiO <sub>2</sub> AND Si <sub>3</sub> N <sub>4</sub> FILMS BY SYNCHROTRON RADIATION AND ITS APPLICATION FOR LOW-TEMPERATURE CLEANING OF Si SURFACES" JOURNAL OF VACUUM SCIENCE AND TECHNOLOGY: PART A, vol. 9, no. 5, 1 September 1991, pages 2653-2661, XP000266450 see page 2657, column 2, paragraph 2 - page 2659, column 2, paragraph 2  -/-	1

☒ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

\* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search

27 April 1999

Date of mailing of the international search report

06/05/1999

Name and mailing address of the ISA  
European Patent Office, P.B. 5818 Patentlaan 2  
NL - 2280 HV Rijswijk  
Tel. (+31-70) 340-2040, Tx. 31 651 epo nl,  
Fax: (+31-70) 340-3016

Authorized officer

Schuermans, N

# INTERNATIONAL SEARCH REPORT

Int'l Application No  
PCT/US 99/00288

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT		
Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	WO 94 23854 A (ENGELSBURG AUDREY C ;CAULDRON LP (US)) 27 October 1994 -----	

# INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No

PCT/US 99/00288

Patent document cited in search report		Publication date	Patent family member(s)	Publication date
DE 4122587 A		23-01-1992	JP 2814021 B	22-10-1998
			JP 4229621 A	19-08-1992
			US 5306671 A	26-04-1992
			KR 9405281 B	15-06-1994
<hr/>				
WO 9423854 A		27-10-1994	AU 684772 B	08-01-1998
			AU 6629794 A	08-11-1994
			BR 9405973 A	12-12-1995
			CA 2160255 A	27-10-1994
			CN 1125917 A	03-07-1996
			CZ 9502671 A	17-04-1996
			EP 0693978 A	31-01-1996
			FI 954837 A	11-10-1995
			HU 73857 A	28-10-1996
			JP 2820534 B	05-11-1998
			JP 8509652 T	15-10-1996
			LV 11288 A	20-06-1996
			LV 11288 B	20-12-1996
			NO 954027 A	11-12-1995
			SG 41949 A	15-08-1997
			US 5643472 A	01-07-1997
			US 5821175 A	13-10-1998
<hr/>				

**THIS PAGE BLANK (USPTO)**